

August 1986 Revised March 2000

DM74LS73A

Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

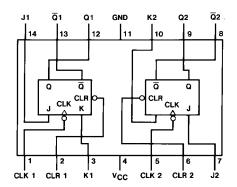
This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. The data on the J and K inputs is allowed to change while the clock is HIGH or LOW without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the levels of the other inputs.

Ordering Code:

Order Number Package Number Package Description				
DM74LS73AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow		
DM74LS73AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide		

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Inputs				Outputs		
CLR	CLK	J	K	Q	Q	
L	Х	Х	Х	L	Н	
Н	\downarrow	L	L	Q_0	\overline{Q}_0	
Н	\downarrow	Н	L	Н	L	
Н	\downarrow	L	Н	L	Н	
Н	\downarrow	Н	Н	Toggle		
Н	Н	Х	Х	Q_0	\overline{Q}_0	

- H = HIGH Logic Level
- L = LOW Logic Level X = Either LOW or HIGH Logic Level
- \downarrow = Negative going edge of pulse. Q_0 = The output logic level before the indicated input conditions were

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Absolute Maximum Ratings(Note 1)

Supply Voltage 7V Input Voltage 7V Operating Free Air Temperature Range $0^{\circ}\text{C to } +70^{\circ}\text{C}$ Storage Temperature Range $-65^{\circ}\text{C to } +150^{\circ}\text{C}$

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V _{CC}	Supply Voltage		4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage		2			V
V _{IL}	LOW Level Input V	oltage			0.8	V
I _{OH}	HIGH Level Output	Current			-0.4	mA
I _{OL}	LOW Level Output	Current			8	mA
f _{CLK}	Clock Frequency (Note 2)		0		30	MHz
f _{CLK}	Clock Frequency (Note 3)		0		25	MHz
t _W	Pulse Width	Clock HIGH	20			
	(Note 2)	Preset LOW	25			ns
		Clear LOW	25			1
t _W	Pulse Width	Clock HIGH	25			
	(Note 3)	Preset LOW	30			ns
		Clear LOW	30			
t _{SU}	Setup Time (Note 2)(Note 4)		20↓			ns
t _{SU}	Setup Time (Note 3)(Note 4)		25↓			ns
t _H	Hold Time (Note 2)(Note 4)		0↓			ns
t _H	Hold Time (Note 3)(Note 4)		5↓			ns
T _A	Free Air Operating Temperature		0		70	°C

Note 2: $C_L = 15$ pF, $R_L = 2$ k Ω , $T_A = 25^{\circ}$ C and $V_{CC} = 5V$.

Note 3: $C_L=50$ pF, $R_L=2$ $k\Omega,\, T_A=25^{\circ}C$ and $V_{CC}=5V.$

Note 4: The symbol (\downarrow) indicates the falling edge of the clock pulse is used for reference.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$				-1.5	V
V _{OH}	HIGH Level Output Voltage	$V_{CC} = Min, I_{OH} = Max$ $V_{IL} = Max, V_{IH} = Min$	2.7	3.4		٧	
V _{OL}	LOW Level Output Voltage	$V_{CC} = Min, I_{OL} = Max$ $V_{IL} = Max, V_{IH} = Min$ $I_{OL} = 4 mA, V_{CC} = Min$			0.35	0.5	٧
					0.25	0.4	
I	Input Current @ Max	V _{CC} = Max	J, K			0.1	
	Input Voltage	$V_I = 7V$	Clear			0.3	mA
			Clock			0.4	
I _{IH}	HIGH Level	V _{CC} = Max	J, K			20	
	Input Current	$V_1 = 2.7V$	Clear			60	μΑ
			Clock			80	
I _{IL}	LOW Level	V _{CC} = Max	J, K			-0.4	
	Input Current	$V_I = 0.4V$	Clear			-0.8	mA
			Clock			-0.8	1
Ios	Short Circuit Output Current	V _{CC} = Max (Note 6)		-20		-100	mA
I _{CC}	Supply Current	V _{CC} = Max (Note 7)			4	6	mA

Note 5: All typicals are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

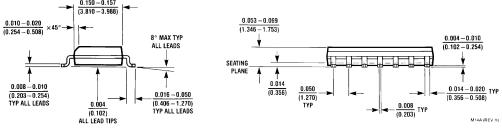
Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state, an equivalent test may be performed where $V_0 = 2.125V$ with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

 $\textbf{Note 7:} \ \ \textbf{With all outputs OPEN, I}_{CC} \ \ \textbf{is measured with the Q and } \ \overline{\textbf{Q}} \ \ \textbf{outputs HIGH in turn.} \ \ \textbf{At the time of measurement, the clock is grounded.}$

Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^{\circ}C$

	Parameter	From (Input)	$R_L = 2 k\Omega$				
Symbol		To (Output)	C _L = 15 pF		C _L = 50 pF		Units
			Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency		30		25		MHz
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		20		28	ns
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to Q		20		24	ns
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or Q		20		24	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\overline{\mathbb{Q}}$		20		28	ns



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A

N144 (REV.E)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770(18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 0.250 ± 0.010 PIN NO. 1 IDENT PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\overline{(7.620 - 8.128)}$ 0.065 $\frac{0.145 - 0.200}{(3.683 - 5.080)}$ 0.060 4° TYP Optional (1.524) (1.651)0.008-0.016 TYP 0.020 (0.203 - 0.406)(0.508) 0.125 - 0.150 0.075 ± 0.015 $\overline{(3.175 - 3.810)}$ 0.280 (1.905 ± 0.381) (7.112) MIN 0.014 - 0.0230.100 ± 0.010 (2.540 ± 0.254) (0.356 - 0.584) $\frac{0.050\pm0.010}{(1.270-0.254)}$ TYP 0.325 ^{+0.040} -0.015 $8.255 + 1.016 \\ -0.381$

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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